LISTING OF CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently Amended) A graphics processor configured to produce data for multiple output buffers, each output buffer associated with a unique output buffer identifier, comprising:

a fragment processing pipeline configured to process graphics data to produce processed graphics data for the multiple output buffers and determine at least one output buffer identifier associated with the processed graphics data, the fragment processing pipeline determining an address associated with the processed fragment data, the address corresponding to a specific location within an output buffer;

a shader read interface configured to read processed graphics data associated with an output buffer identifier from an output buffer stored in a memory; [[and]]

a write interface configured to write processed graphics data associated with at least one output buffer identifier to an output buffer stored in the memory; and

wherein the graphics data includes fragment data including at least two fragments within a single surface, the fragment processing pipeline being configured to separate the at least two fragments and write each of the fragments to a separate one of the output buffers.

Claim 2 (Original) The graphics processor of claim 1, further comprising a geometry processor configured to process graphics data.

Claim 3 (Cancelled)

Claim 4 (Previously Presented) The graphics processor of claim 1, wherein an output buffer includes data represented in two or more data formats including fixed point and floating point or including different numbers of bits within the same output buffer.

Claim 5 (Original) The graphics processor of claim 1, wherein the output buffer identifier is readable and writable by the fragment processing pipeline.

Claim 6 (Previously Presented) The graphics processor of claim 1, wherein any of the multiple output buffers is selected for display using the address defined in the fragment processing pipeline.

Claim 7 (Original) The graphics processor of claim 1, wherein the fragment processing pipeline includes multiple registers, each register capable of outputting data to one or more of the multiple output buffers.

Claim 8 (Cancelled)

Claim 9 (Original) The graphics processor of claim 1, wherein the graphics processor resides within a computing system including a host processor.

Claim 10 (Cancelled)

Claim 11 (Currently Amended) The ~~method of claim 10, further comprising~~ graphics processor of claim 1 wherein:

~~reading~~ the processed fragment data is read from the output buffer using the output buffer identifier.

Claim 12 (Currently Amended) The ~~method of claim 10~~ graphics processor of claim 1, wherein the processed fragment data stored in the output buffer includes fragment depth data.

Claims 13-15 (Cancelled)

Claim 16 (Currently Amended) The ~~method of claim 10~~ graphics processor of claim 1, wherein the processed fragment data stored in the output buffer includes displaced mesh data, the ~~method including displacing~~ processor being adapted to displace the processed fragment data to produce one or more displaced meshes, and storing each of the displaced meshes in one of the multiple output buffers.

Claims 17-20 (Cancelled)

Claim 21 (Previously Presented) The graphics processor of claim 1, wherein the output buffer includes data having different multi-bit formats including 16-bit and 32-bit formats within the same output buffer.

Claim 22 (Cancelled)

Claim 23 (Currently Amended) The graphics processor of claim [[22]] 1, wherein the fragment processing pipeline is configured to select one of the output buffers for writing each of the fragments based on a procedurally computed function.

Claim 24 (Currently Amended) ~~The graphics processor of claim 1,~~ A graphics processor configured to produce data for multiple output buffers, each output buffer associated with a unique output buffer identifier, comprising:

a fragment processing pipeline configured to process graphics data to produce processed graphics data for the multiple output buffers and determine at least one output buffer identifier associated with the processed graphics data, the fragment processing pipeline determining an address associated with the processed fragment data, the address corresponding to a specific location within an output buffer;

a shader read interface configured to read processed graphics data associated with an output buffer identifier from an output buffer stored in a memory;

a write interface configured to write processed graphics data associated with at least one output buffer identifier to an output buffer stored in the memory;

wherein the fragment processing pipeline is configured to process the graphics data of at least two fragments in parallel, the fragment processing unit determining the destination address in one of the output buffers for each of the fragments; and

wherein the fragment processing pipeline is configured to respond to a flush instruction to avoid read after write conflicts when reading from one of the output buffers that can be accessed by the processing pipeline, the graphics processor responding to a write instruction to indicate that all pending write operations are complete.

Claim 25 (Cancelled)

Claim 26 (Currently Amended) ~~The graphics processor of claim 1,~~ A graphics processor configured to produce data for multiple output buffers, each output buffer associated with a unique output buffer identifier, comprising:

a fragment processing pipeline configured to process graphics data to produce processed graphics data for the multiple output buffers and determine at least one output buffer identifier associated with the processed graphics data, the fragment processing pipeline determining an address associated with the processed fragment data, the address corresponding to a specific location within an output buffer;

a shader read interface configured to read processed graphics data associated with an output buffer identifier from an output buffer stored in a memory;

a write interface configured to write processed graphics data associated with at least one output buffer identifier to an output buffer stored in the memory;

wherein the fragment processing pipeline is configured to process graphics data to produce visible fragment data for visible fragments;

one of the multiple output buffers stores depth map values of the visible fragments;

[[one]] two or more of the output buffers store fragment data; and

the graphics processor further includes a shader for shading the visible fragments using the portion of the fragment data read from the one or more of the output buffers and the depth map read from one of the output buffers.

Claim 27 (Previously Presented) The method of claim 12, wherein the processed fragment data includes visible fragment data for visible fragments;

one of multiple output buffers stores the depth map data of the visible fragments; and

shading the visible fragments using the portion of the fragment data read from the one or more additional output buffers and the depth map data read from one of the output buffers.

Claim 28 (Previously Presented) The method of claim 27, wherein each of the displaced meshes is used as a vertex array to animate geometry.

Claim 29 (Previously Presented) The method of claim 28, further including displacing the processed fragment data along a normal vector to produce the displaced meshes.